

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

[Search Results](#)[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "'('integrated circuit' and 'logic cone' and delay)<in>metadata)'"

[e-mail](#)

Your search matched 1 of 1227909 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)[New Search](#)

Modify Search

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

- ☐ 1. Statistically estimating path delay fault coverage in combinational circuit
Zhang, Z.; McLeod, R.D.; Miller, D.M.; Zhang, S.;
Communications, Computers, and Signal Processing, 1995. Proceedings. IEEE
Conference on
17-19 May 1995 Page(s):461 - 464
Digital Object Identifier 10.1109/PACRIM.1995.519569
[AbstractPlus](#) | Full Text: [PDF](#)(308 KB) IEEE CNF

Indexed by
 Inspec[Help](#) [Contact Us](#) [Privacy & :](#)

© Copyright 2005 IEEE -